WHAT IS CLAIMED IS:

1. A method of evaluating the quality of test sequences for delay faults configured in such manner that:

of all defined delay faults, the delay faults having delay values equal to or lower than a predetermined design delay value are excluded from a test object; and

a ratio of "the number of the delay faults detected by the test sequences for delay faults" to the number of the remaining delay faults to be tested is set as a fault coverage, thereby evaluating the quality of the "test sequences for delay faults".

2. A method of evaluating the quality of test sequences for delay faults including steps of:

excluding, of all defined delay faults, the delay faults having delay values equal to or lower than a predetermined design delay value from a test object;

calculating a ratio of "the number of the delay faults detected by the test sequences for delay faults" to the number of the remaining delay faults to be tested according to the excluding step as a fault coverage; and

evaluating the quality of the "test sequences for delay faults" based on the fault coverage.

3. A method of evaluating the quality of test sequences for delay faults configured in such manner that:

each of defined delay faults is weighted; and

a ratio of the total of the weights with respect to the "delay faults detected by the test sequences for delay faults" to the total of the weights with respect to the defined delay faults is set as a fault coverage, thereby evaluating the quality of the "test sequences for delay faults".

4. A method of evaluating the quality of test sequences for delay faults including steps of:

weight each of defined delay faults;

calculating a ratio of the total of the weights with respect to the "delay faults detected by the test sequences for delay faults" to the total of the weights with respect to the defined delay faults as a fault coverage; and

evaluating the quality of the "test sequences for delay faults" based on the fault coverage.

5. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 3 configured in such manner that a relative value of a "design delay value on a signal path on which a delay fault is defined" with respect to a "timing design request value on the delay fault defined signal path" is used as the weight.

6. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 5 configured in such manner that a clock rate with respect to the delay fault defined signal path is used for the "timing design request value on the delay fault defined signal path".

7. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 3 configured in such manner that a "gate stage number with respect to the delay fault defined signal path" is used as the weight.

8. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 3 configured in such manner that the product of the "design delay value on the delay fault defined signal path" and a "physical path length on the delay fault defined signal path" is used as the weight.

9. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 3 configured in such manner that the product of the "design delay value on the delay fault defined signal path" and a "physical wiring area on the delay fault defined signal path" is used as the weight.

10. A method of evaluating the quality of test sequences

for delay faults as claimed in Claim 3 configured in such manner that the product of the "design delay value on the delay fault defined signal path" and the sum of a "physical path area on the delay fault defined signal path" and an element area thereon is used as the weight.

11. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 7 configured in such manner that a defect density is further used for multiplication as the weight.

12. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 8 configured in such manner that a defect density is further used for multiplication as the weight.

13. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 9 configured in such manner that a defect density is further used for multiplication as the weight.

14. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 10 configured in such manner that a defect density is further used for multiplication as the weight.

15. A method of evaluating the quality of test sequences for delay faults configured in such manner that the "method of evaluating the quality of test sequences for delay faults" as claimed in Claim 1 is applied to the generated "test sequences for delay faults", to thereby calculate a fault coverage.

16. A method of evaluating the quality of test sequences for delay faults configured in such manner that the "method of evaluating the quality of test sequences for delay faults" as claimed in Claim 3 is applied to the generated "test sequences for delay faults", to thereby calculate a fault coverage.

17. A method of simulating the quality of test sequences for delay faults configured in such manner that the "method

of evaluating the quality of test sequences for delay faults" as claimed in Claim 1 is applied to the given "test sequences for delay faults", to thereby calculate a fault coverage.

18. A method of simulating the quality of test sequences for delay faults configured in such manner that the "method of evaluating the quality of test sequences for delay faults" as claimed in Claim 3 is applied to the given "test sequences for delay faults", to thereby calculate a fault coverage.

19. A method of testing faults configured in such manner that the "method of evaluating the quality of test sequences for delay faults" as claimed in Claim 1 is applied to the "test sequences for delay faults" used for a test in testing steps for a semiconductor integrated circuit, to thereby calculate a fault coverage.

20. A method of testing faults configured in such manner that the "method of evaluating the quality of test sequences for delay faults" as claimed in Claim 3 is applied to the "test sequences for delay faults" used for a test in testing steps of a semiconductor integrated circuit, to thereby calculate a fault coverage.

21. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 3 configured in such manner that a ratio of the "design delay value on the delay fault defined signal path" to the "timing design request value on the delay fault defined signal path" is used as the weight.

22. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 21 configured in such manner that the clock rate with respect to the delay fault defined signal path is used for the "timing design request value on the delay fault defined signal path".

23. A method of evaluating the quality of test sequences for delay faults as claimed in Claim 21 configured in such manner that, when the delay fault defined signal path is a

multicycle path, the product of the clock rate with respect to the delay fault defined signal path and the number of the multicycles is used for the "timing design request value on the delay fault defined signal path".